

# SINGLE PHASE PV CELL FED H- BRIDGE MULTILEVEL INVERTER USING BOOST CONVERTER

M. Kavitha\*, A. Arunkumar\*\*, N. Gokulnath\*\*, S. Arun \*\* and A. Ragavendiran\*

\*Assistant Professor/ Dept. of Electrical & Electronics Engineering

\*\*B.tech students / Dept. of EEE / DR.S.J.S Paul Memorial College of Engineering & Technology / Pondicherry / India

3) Cascaded H-bridge inverter (multilevel cascade)

**Abstract**— This paper presents a single-phase five-level photovoltaic (PV) inverter topology for grid-connected PV systems with a Sinusoidal Pulse Width-Modulated (SPWM) control scheme. The photo-voltaic arrays are connected to five-level multilevel inverter through the DC-DC boost converter. By implementing maximum power point tracking algorithm are producing more power from PV array. The DC power from the PV array is boosted by using the DC-DC boost converter. The boosted DC supply is applied to PWM inverter which is controlled by PI controller. MATLAB/SIMULINK platform are used to simulate the circuit operation and control signal. The results show that cascaded H-bridge multilevel inverter with pv cell.

**Keywords**— Photovoltaic Cells, Maximum Power Point Tracking, Boost Converter, Cascaded H-Bridge Multilevel Inverter .

## 1. INTRODUCTION

The demand for renewable energy has increased significantly over the years because of shortage of fossil fuels and greenhouse effect. Among various types of renewable energy sources, solar energy and wind energy have become very popular and demanding due to modern technology world. PV sources are used today in many advantages such as free from pollution. Solar-electric-energy demand has grown consistently by 20% - 25% per annum over the past 20 years, which is mainly due to the decreasing costs and prices [1]. PV inverter is used to convert dc power obtained from PV modules into ac power to be fed into the load. Improving the output waveform and performance of the inverter reduces its respective harmonic content and, hence the size of the

filter used and the level of electromagnetic interference (EMI) generated by switching operation of the inverter [2]. In recent years, multilevel inverters have become more attractive for researchers and manufacturers due to their advantages over conventional three-level pulse width-modulated (PWM) inverters. They offer improved output waveforms, smaller alter size, lower EMI, lower total harmonic distortion (THD) [3- 4].

The three common topologies for multilevel inverter are:

- 1) Diode clamped (neutral clamped)
- 2) Capacitor clamped (dying capacitors)

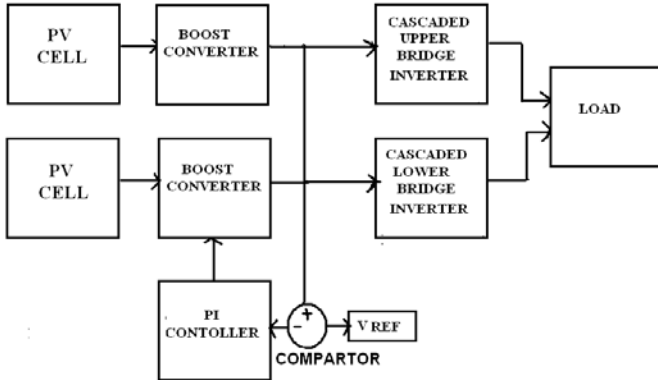
Several modulation and control strategies have been developed for multilevel inverters like multilevel sinusoidal (PWM), multilevel selective harmonic elimination, and space-vector modulation [3]. A typical single-phase three-level inverter adopts full-bridge configuration by using approximate sinusoidal modulation technique as the power circuits. The output voltage has zero,  $V_{dc}$  and  $V_{dc}$  supply dc voltage. The harmonic components of the output voltage are determined by the carrier frequency and switching functions. Therefore, their harmonic reduction is limited to a certain degree [4].

To overcome, this paper presents a five-level PWM inverter whose output voltage can be represented in the following five levels: zero,  $+V_{dc}/2$ ,  $V_{dc}$ ,  $-V_{dc}/2$ , and  $-V_{dc}$ . As the number of output levels increases, the harmonic content can be reduced. This inverter topology uses two reference signals, instead of one reference signal, to generate PWM signals for the switches. Both the reference signals  $V_{ref1}$  and  $V_{ref2}$  are identical to each other, except for an offset value equivalent to the amplitude of the carrier signal  $V_{carrier}$ . Because the inverter is used in a PV system, a PI current control scheme is employed to keep the output current sinusoidal and to have high dynamic performance under rapidly changing atmospheric conditions and to maintain the power factor at near unity. Simulation results are presented to validate the proposed inverter configuration.

## 2. PROPOSED CONCEPT

The proposed concept consists of the single phase PV cell are connected to a H-Bridge Multilevel Inverter using a boost converter. Maximum Power Point Tracking (MPPT) is implemented in solar array power system with direct control method. The incremental conductance algorithm is used to track the Maximum Power Point tracking, as it performs better control under rapidly changing atmospheric condition. Boost converter can step up the voltage without using a transformer. In multilevel inverter use of two dc sources with the 8 switches instead of 16 switches for conventional H bridge inverter to get required five level output voltage and to reduce the harmonics. The main disadvantage of conventional H bridge inverter is input voltage is fixed to over this problem, in the proposed

prototype boost converter is used to regulate and to obtain the desired input voltage and further the DC source is replaced by a renewable resource such as solar panels, fuel cell to get desired DC voltage to grid connected system In this paper there will be two inputs one is from Fuel cell and other is from PV array. 12V is taken from PV cell and PV array and then they are boosted to a voltage from 115V to 230V respectively by using boost converter. Finally a five-level output is observed by giving the two supply voltages to the



multilevel inverter. The general configuration of proposed circuit is shown in Fig 1.

Fig 1: General Configuration of proposed circuit

### 3. Methodology

#### 3.1 PV ARRAY

Photons of light with energy higher than the band-gap energy of PV material can make electrons in the material break free from atoms that hold them and create electron and hole pairs. These electrons however, will soon fall back into holes causing charge carriers to disappear. If a nearby electric field is provided, those in the conduction band can be continuously swept away from holes toward a metallic contact where they will emerge as an electric current. The electric field within the semiconductor itself at the junction between two regions of crystals of different type, called a p-n junction. The PV cell has electrical contacts on its top and bottom to capture the electrons. When the PV cell delivers power to the load, the electrons flow out of the n-side into the connecting wire, through the load, and back to the p-side where they recombine with holes [4]. Note that conventional current flows in the opposite direction from electrons.

#### 3.2 PV Model

The use of equivalent electric circuits makes it possible to model characteristics of a PV cell. The m-file coding are implemented in MATLAB programs for simulations. The below Fig. 2 shows M-File coding model of solar cell. It is used to vary the input voltage according to variation in temperature.

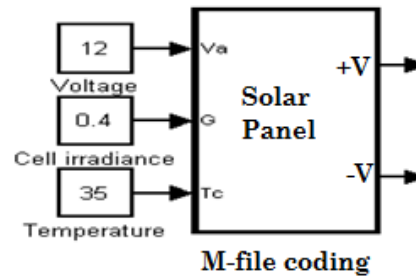


Fig. 2: M-file coding model of Solar cell

M-File coding is given in below:

```
function Ia=solar(Va,Suns,TaC)
k = 1.38e-23;
q = 1.60e-19;
n=2;
vg= 1.12;
Ns = 36;
T1 = 273 + 25;
Voc_T1 = 21.06/Ns;
Isc_T1 = 3.80;
T2 = 273 + 75;
Voc_T2 = 17.05/Ns;
Isc_T2 = 3.92;
TaC=25;
Suns=1;
TaK = 273 + TaC;
KO = (Isc_T2 - Isc_T1)/(T2 - T1);
IL_T1 = Isc_T1 * Suns;
IL = IL_T1 + KO*(TaK - T1);
IO_T1 = Isc_T1/(exp(q*Voc_T1/(n*k*T1))-1);
IO = IO_T1*(TaK/T1).^(3/n).*exp(-q*vg/(n*k)).*((1/TaK)-(1/T1));
Xv = IO_T1*q/(n*k*T1) * exp(q*Voc_T1/(n*k*T1));
dVdI_V0c = - 1.15/Ns /2;
Rs = - dVdI_V0c - 1/Xv;
A=0.8
Va=0:8
Vt_Ta = A * k * TaK / q; % = A * kT/q
Vc = Va/Ns;
Ia = zeros(size(Vc));
for j=1:5;
Ia = Ia-(IL - Ia -IO.*(exp((Vc + Ia.*Rs)/Vt_Ta)-1)) /
(-1 - (IO.*(exp((Vc+Ia.*Rs)/Vt_Ta) -1)).*Rs./Vt_Ta);
end
plot(Ia)
for i=1:8
P(i)=Va(i)*Ia(i);
End
```

where

- $R_s$  = Series Resistance of the cell
- $V_{tc}$  = Thermal potential at working temperature
- $I_o$  = Reverse saturation current at working temperature
- $V_c$  = cell voltage per cell
- $I_a$  = output current of the cell
- $I_{sc}$  = short circuit current
- $I_{sck}$  = short circuit current at reference temperature
- $T_{ak}$  = Cell temperature in Kelvin
- $T_{ref}$  = Reference Temperature (25 C) in Kelvin
- $I_{ok}$  = Reverse saturation current at reference temperature

### 3.3 PV CHARACTERISTICS

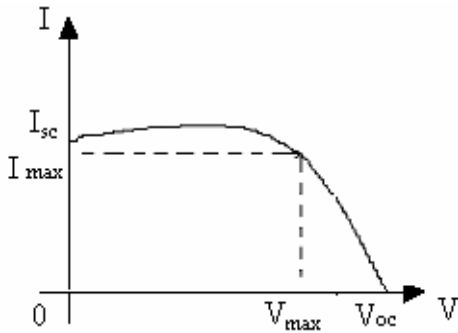


Fig. 3: Output Characteristics Of Solar cell

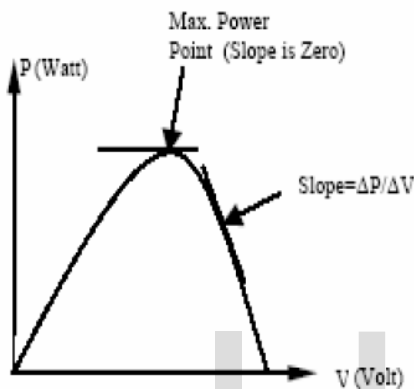


Fig. 4: P-V characteristics of Solar cell

The output characteristics of a solar cell is shown in Fig. 3 and the Fig. 4 shows the typical Power versus Voltage curve of the PV array. In this figure, P is the power extracted from PV array and V is the voltage across the terminals of the PV array. The characteristics have different slopes at various points. When maximum power is extracted from PV array the system is operating at MPPT where slope is zero.

### 4. MPPT

Maximum power point tracking (MPPT) is a technique that grid-tie inverters, solar battery chargers and similar devices use to get the maximum possible power from one or more photovoltaic devices, typically solar panels, though optical power transmission systems can benefit from similar technology. Solar cells have a complex relationship between solar irradiation, temperature and total resistance that produces a non-linear output efficiency known as the I-V curve. It is the purpose of the MPPT system to sample the output of the cells and apply the proper resistance (load) to obtain maximum power for any given environmental conditions. MPPT devices are typically integrated into an electric power converter system that provides voltage or

current conversion, filtering, and regulation for driving various loads, including power grids, batteries, or motors.

### 4.1 MPPT V-I CURVE IN VARYING SUNLIGHT

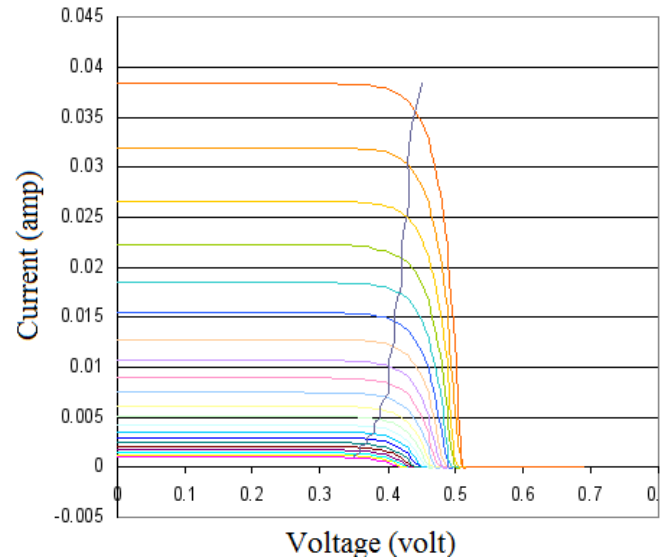


Fig. 5: MPPT V-I curve in varying sunlight

The MPPT V-I curve in varying in sunlight is shown in Fig. 5. Photovoltaic cells have a complex relationship between their operating environment and the maximum power they can produce. The fill factor, abbreviated FF, is a parameter which characterizes the non-linear electrical behavior of the solar cell. Fill factor is defined as the ratio of the maximum power from the solar cell to the product of Open Circuit Voltage  $V_{oc}$  and Short-Circuit Current  $I_{sc}$ . In tabulated data it is often used to estimate the maximum power that a cell can provide with an optimal load under given conditions,  $P = FF * V_{oc} * I_{sc}$ . For most purposes, FF,  $V_{oc}$ , and  $I_{sc}$  are enough information to give a useful approximate model of

the electrical behavior of a photovoltaic cell under typical conditions. For any given set of operational conditions, cells have a single operating point where the values of the current (I) and Voltage (V) of the cell result in a maximum power output. These values correspond to a particular load resistance, which is equal to  $V / I$  as specified by Ohm's Law. The power P is given by  $P = V * I$ .

A photovoltaic cell, for the majority of its useful curve, acts as a constant current source. However, at a photovoltaic cell's MPP region, its curve has an approximately inverse exponential relationship between current and voltage. From basic circuit theory, the power delivered from or to a device is optimized where the derivative (graphically, the slope)  $dI/dV$  of the I-V curve is equal and opposite the  $I/V$  ratio (where  $dP/dV = 0$ ). This is known as the maximum power point (MPP) and corresponds to the "knee" of the curve.

A load with resistance  $R=V/I$  equal to the reciprocal of this value draws the maximum power from the device. This is sometimes called the characteristic resistance of the cell. This is a dynamic quantity which changes depending on the level of illumination, as well as other factors such as temperature and the age of the cell.

If the resistance is lower or higher than this value, the power drawn will be less than the maximum available, and thus the cell will not be used as efficiently as it could be. Maximum power point trackers utilize different types of control circuit or logic to search for this point and thus to allow the converter circuit to extract the maximum power available from a cell.

### 4.2 TYPES OF MPPT ALGORITHM METHOD

Tracking the maximum power point of a photovoltaic array is usually an essential part of a PV system. As such many MPP tracking methods have been developed and implemented. The problem considered by MPPT techniques is to automatically find the voltage  $V_{MPP}$  or current  $I_{MPP}$  at which a PV array should operate to obtain the maximum power output  $P_{MPP}$  under a given temperature and irradiance.

The various MPPT methods are:

1. Perturb and observe (P&O) method
2. Incremental conductance method

MPPT technique	speed	Complexity	Periodic tuning	Sensed parameters
Perturb and observe	Varies	Low	No	Voltage
Incremental Conductance	Varies	Medium	No	Voltage, Current

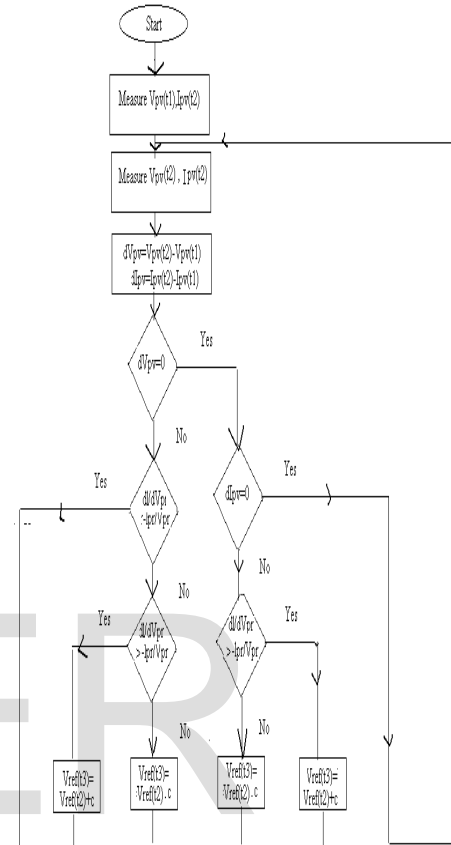
Table 1  
 Characteristics of different MPPT Technique

The incremental conductance algorithm is used to track the MPPT, as it performs better control under rapidly changing atmospheric condition. So incremental conductance method is used in this proposed method.

#### 4.2.1 Incremental Conductance method

The flow chart of Incremental conductance method is shown in the Fig1.6. The Incremental conductance algorithm states that when the operating voltage of the PV panel is perturbed by a small increment, if the resulting change in power  $P$  is positive, then we are going in the direction of MPP and we keep on perturbing in the same direction. If  $P$  is negative, we are going away from the direction of MPP and the sign of perturbation supplied has to be changed. However, in this algorithm we use only one sensor, that is the voltage

sensor, to sense the PV array voltage and so the cost of implementation is less and hence easy to implement. The time complexity of this algorithm is very less but on reaching very close to the MPP it doesn't stop at the MPP and keeps on perturbing in both the directions. When this happens the algorithm has reached very close to the MPP and we can set an appropriate error limit or can use a wait function which ends up



increasing the time complexity of the algorithm.

shows a simplified schematic of the boost power stage.

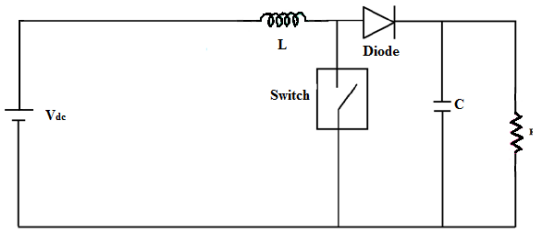


Fig.1.6:  
Flow  
chart of

Incremental conductance method

Fig.1.7: Boost Power Stage Schematic

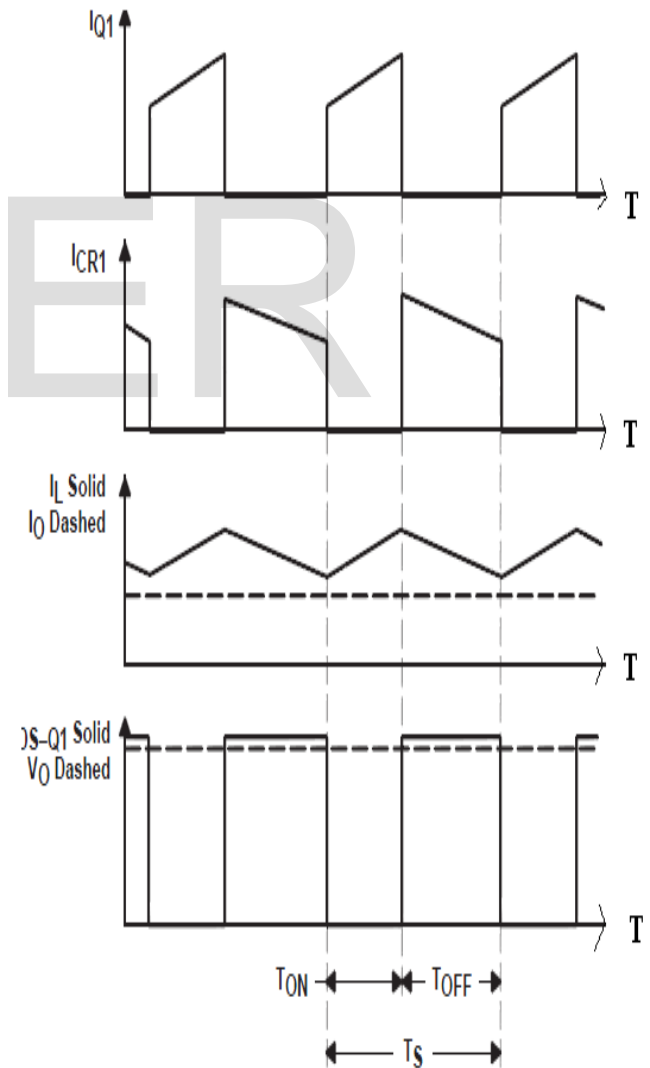
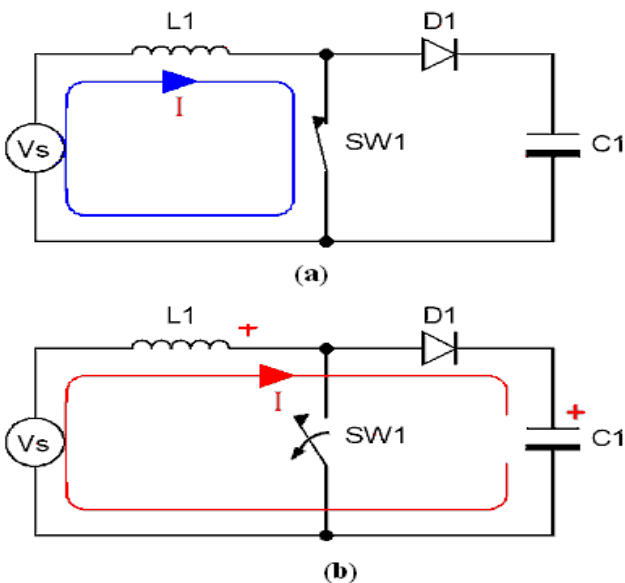
### 5 DC-DC CONVERTERS

The DC-DC converters are used as switching mode regulators to convert an unregulated dc voltage to a regulated dc output voltage. The regulation is normally achieved by PWM at a fixed frequency and the switching device is generally BJT, MOSFET or IGBT. The minimum oscillator frequency should be about 100 times longer than the transistor switching time to maximize efficiency. This limitation is due to the switching loss in the transistor. The transistor switching loss increases with the switching frequency and thereby, the efficiency decreases. The core loss of the inductors limits the high frequency operation. Control voltage  $V_C$  is obtained by comparing the output voltage with its desired value. Then the output voltage can be compared with its desired value to obtain the control voltage  $V_{Cr}$ . The PWM control signal for the dc converter is generated by comparing  $V_C$  with a saw tooth voltage  $V_T$ [8]. There are four topologies for the switching regulators: buck converter, boost converter, buck-boost converter, cuk converter. However my project work deals with the boost regulator and further discussions will be concentrated towards this one . Fig. 5

### 5.1 Basic principle for boost converter

#### MODE 1 :

The basic operation of boost converter when switches is closed is shown in Fig 1.8 (a).When the switch is closed the inductor gets charged through the battery and stores the energy. In this modes inductor current rises but for simplicity





we assume that the charging and the discharging of the inductor are linear. The diode blocks the current flowing and so the load current remains constant which is being supplied due to the discharging of the capacitor .

**MODE 2 :**

The basic operation of boost converter when switches is open is shown in Fig 1.8 (b).In mode 2 the switch is open and so the diode becomes short circuited. The energy stored in the inductor gets discharged through opposite polarities with charge the capacitor. The load current remains constant throughout the operation.

Fig 1.8: basic operation of boost converter

**5.2 WAVEFORM OF BOOST CONVERTER**

The output for the boost converter is given in the Fig 1.9The boost converter is a popular non-isolated power stage topology, sometimes called a step-up power stage. Power supply designers choose the boost power stage because the required output is always higher than the input voltage. The input current for a boost power stage is continuous, or non-pulsating, because the output diode conducts only during a portion of the switching cycle. The output capacitor supplies the entire load current for the rest of the switching cycle. Inductor L and capacitor C make up the effective output filter. The capacitor equivalent series resistance (ESR),  $R_c$ , and the inductor dc resistance,  $R_L$ , are included in the analysis. Resistor(R) represents the load seen by the power supply output. A power stage can operate in continuous or discontinuous inductor current mode. In continuous inductor current mode, current flows continuously in the inductor

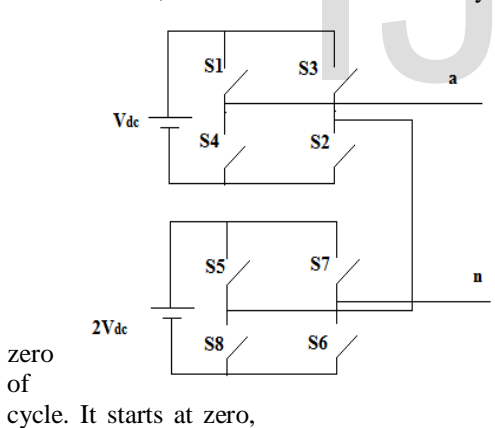


Fig.1.9: Output for Boost converter

reaches peak value, and return to zero during each switching cycle. It is desirable for a power stage to stay in only one mode over its expected operating conditions because the power stage frequency response changes significantly between the two modes of operation.

**5.3 DESIGN OF BOOST CONVERTER**

The Duty cycle (D) can be given as,

$$D = 1 - \frac{V_{in(min)} * \eta}{V_{out}} \tag{1}$$

Where  $V_{in(min)}$  is the minimum input voltage,  $V_{out}$  is the desired output voltage, and  $\eta$  is the efficiency of the converter.

The inductor ripple current ( $\Delta I_L$ ) can be given as

$$\Delta I_L = (0.2 \text{ to } 0.4) * I_{OUT(max)} * \frac{V_{out}}{V_{in}} \tag{2}$$

The inductor (L) can be given as,

$$L = \frac{V_{in} * (V_{out} - V_{in})}{\Delta I_L * f_s * V_{out}} \tag{3}$$

**6 CACADED H BRIDGE MULTILEVEL INVERTER**



Fig. 10 : Cascaded H-bridge multilevel inverter

The diagrammatic representation for the cascaded H-bridge multilevel inverter is shown in the Fig 1.10. The output waveform of five level multilevel inverter is shown in Fig1.11 The main advantages of the cascaded multilevel inverter are that the regulation of the DC buses is simple. Modularity of control can be achieved. Unlike the diode clamped and capacitor clamped inverter where the individual phase legs must be modulated by a central controller, the full-bridge inverters of a cascaded structure can be modulated separately. Requires the least number of components among all multilevel converters to achieve the same number of voltage levels. Soft-switching can be used in this structure to avoid bulky and lossy resistor-capacitor-diode snubbers. To overcome the demerits of the other types of the multilevel inverter the cascaded H-bridge multilevel inverter have been used in this work.

Fig. 11: Output of cascaded H-bridge multilevel inverter

**6.1 OPERATION MODES OF MULTILEVEL INVERTER**

The cascaded H-bridge multilevel inverter reduces the cost of the inverter. The operation of the cascaded H-bridge multilevel inverter can be explained. The converter topology is based on the series connection of single-phase inverters with separate dc sources. The resulting phase voltage is synthesized by the addition of the voltages generated by the different cells. In a 3-level cascaded inverter each single-phase full-bridge inverter generates three voltages at the output:  $+V_{dc}$ , 0,  $-V_{dc}$  (zero, positive dc voltage, and negative dc voltage). This is made possible by connecting the capacitors sequentially to the ac side via the power switches. The resulting output ac voltage swings from  $-V_{dc}$  to  $+V_{dc}$  with three levels,  $-2V_{dc}$  to  $+2V_{dc}$  with five-level [15]. The operation modes of five level cascaded H bridge multilevel inverter is shown in Table 2.

TABLE 2  
OPERATION MODES OF FIVE LEVEL INVERTER

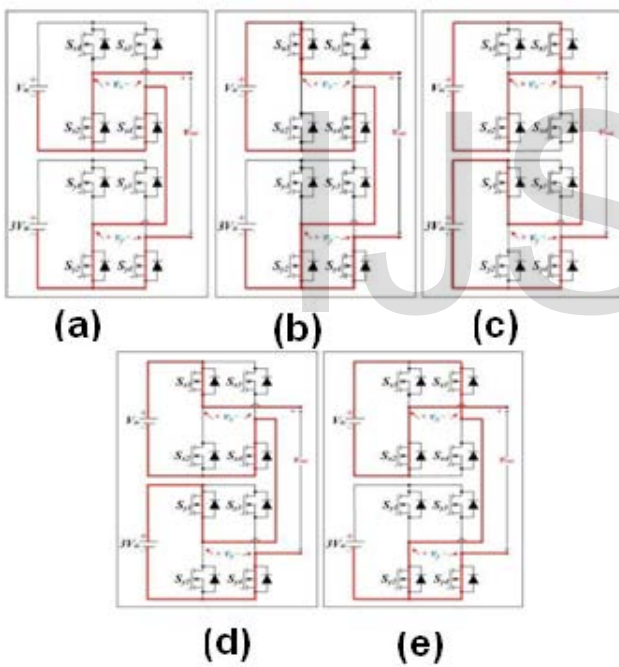
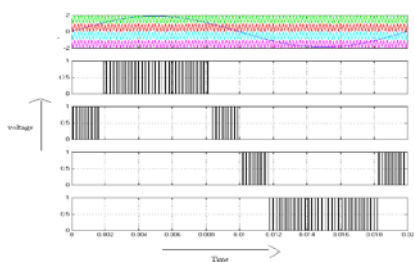


Fig. I.12.:Operational mode to produce output voltage

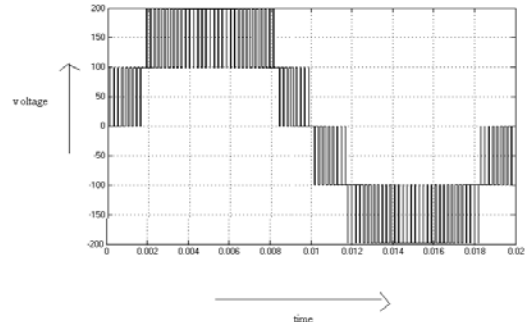


l  
e  
v  
e  
l  
s  
,  
(  
a

) 0-level, (b)  $V_{dc}$ , (c)  $2V_{dc}$ , (d)  $-V_{dc}$ , (e)  $-2V_{dc}$ ,

**6.2. Switching patterns of the proposed single phase five-level PWM inverter**

There are two PWM methods mainly be used in multilevel inverter control strategy. One is fundamental



switching frequency and another one is high switching frequency. High switching frequency can be classified as space vector PWM, selective harmonics elimination PWM and Sinusoidal Pulse Width modulation (SPWM). Among these PWM methods SPWM is the mostly used for multilevel inverter, because it has very simple and easy to implement. SPWM method can be classified as follows. They are Phase

OPERATION	0	$V_{DC}$	$2V_{DC}$	$-V_{DC}$	$-2V_{DC}$
S1	OFF	ON	OFF	OFF	OFF
S2	OFF	ON	OFF	OFF	OFF
S3	OFF	OFF	ON	OFF	OFF
S4	OFF	OFF	ON	OFF	OFF
S5	OFF	OFF	OFF	ON	OFF
S6	OFF	OFF	OFF	ON	OFF
S7	OFF	OFF	OFF	OFF	ON
S8	OFF	OFF	OFF	OFF	ON

Disposition PWM (PDPWM), Phase Opposition Disposition PWM (PODPWM), and Alternative Phase Opposition Disposition PWM (APODPWM)[12]. It is generally accepted that the phase disposition strategy gives rise to the lowest harmonic distortion for the line-line voltage. So PDPWM control strategy is used in this work.

**6.2.1 Phase Disposition Pulse width modulation**

The rules for the phase disposition PWM method, when the number of level  $n=5$ , are given below

ig.1.13: Switching pattern for PDPWM

### 6.3 MODELLING OF SINGLE PHASE FIVE LEVEL CASCADED H- BRIDGE INVERTER

For each full bridge inverter the output voltage is given by

$$V_{0i} = V_{dc} (S1i - S2i) \tag{4}$$

And the input dc current is

$$I_{dci} = I_a (S1i - S2i) \tag{5}$$

Where,

- (a)  $i = 1 \dots 5$  (number of full bridge inverters employed) for the 5 level type.
- (b)  $I_{am}$  is the output current of the cascaded inverter.
- (c)  $S1i$  and  $S2i$  is the upper switch of each full bridge inverter.

Now the output voltage of each phase of the multilevel cascaded inverter is given by:

$$V_{on} = \sum V_{0i} \quad i = 1, 2, \dots, n \tag{6}$$

In multilevel inverters, the amplitude modulation index ( $m_a$ ) is the ratio of reference amplitude ( $a_M$ ) to carrier amplitude ( $A_c$ ).

$$m_a = A_m / (m-1) A_c \tag{7}$$

The frequency ratio ( $m_f$ ) is ratio of carrier frequency ( $f_c$ ) to reference frequency ( $f_m$ ).

$$m_f = f_c / f_m \tag{8}$$

## 7. CONTROLLERS

A controller is a device that generates an output signal based on the input signal it receives. The input signal is actually an error signal, which is the difference between the measured variable and the desired value or set point. The basic block diagram of controllers is shown in Fig 1.14 .

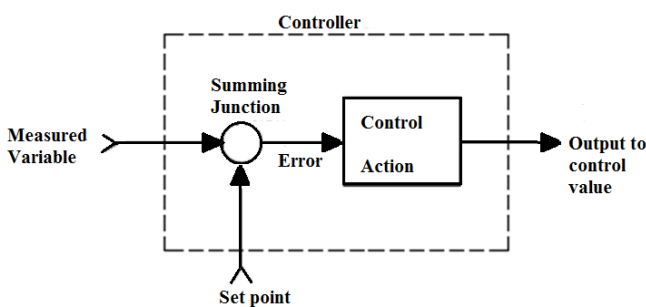


Fig.1.14: Structure of a controller

### 7.2 PI controller

PI controller forms control signal in the following way:

$$u(t) = \left[ e(t) + \frac{1}{T_i} \int_0^t e(\tau) d\tau \right] \tag{9}$$

where  $T_i$  is the integral time constant of PI controller. This can be graphically shown in the Fig. 1.11 by assuming  $K=1$  and  $T_i=1$ . Constant  $K_i = \frac{K}{T_i}$  is called "reset mode". Integral controller is also sometimes called as reset control.

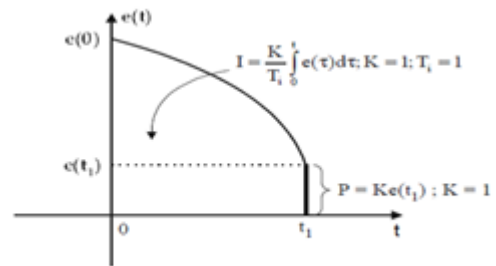


Fig.1.15: PI controller signal generation

The waveform PI controller signal generation is given in the Fig. 1.11. The name comes from the term "manual reset" which marks a manual change of operating point or of "bias"  $u_0$  in order to eliminate error. PI controller performs this function automatically. If control signal of P controller in proportional area is compared with PI controller output signal it can be seen that constant signal  $u_0$  is replaced with signal proportional with the area under error curve.

$$u_0 = \frac{K}{T_i} \int_0^t e(\tau) d\tau \tag{10}$$

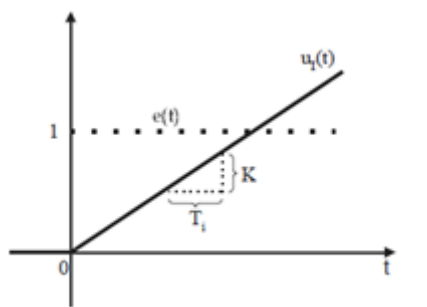
The fact that  $u_0$  is replaced with an integral allows PI controller to eliminate steady state error. On the other hand, P controller cannot eliminate steady state error since it does not have any algorithm that would allow for the controller to increase control signal  $u(t)$  in order to increase controlled variable  $y(t)$  (assuming positive process gain) if in some moment  $t_1$  error  $e(t_1) = \text{const.} > 0$ . Proportional control law stays constant in this case and it will not try to change a controlled variable in such manner that control error is diminished.

PI controller on the other hand will increase control signal when error  $e(t_1) = \text{const.} > 0$ . To the proportional part of the signal will be added integral part proportional to the area under curve  $e(t)$ , so, overall signal will be bigger.

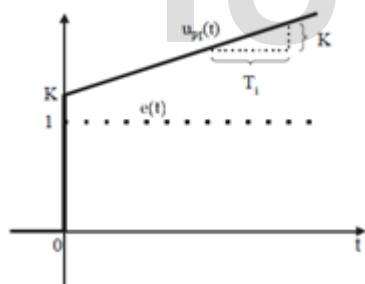
$$u(t) = Ke(t) + \frac{K}{T_i} \int_0^t e(\tau) d\tau = u_p(t) + u_i(t) \tag{11}$$



Assuming positive process gain, increase in control signal will result in increase in controlled variable and error will tend toward zero. When  $e(t) < 0$ , control signal will decrease, control variable will also decrease and error will tend toward zero. PI controller will not be active only when  $e(t) = 0$ . In all other situations PI controller will act to lead steady state control error to zero. It can be concluded that PI controller will eliminate forced oscillations and steady state error resulting in operation of on-off controller and P controller respectively. However, introducing integral mode has a negative effect on speed of the response and overall stability of the system. PI controllers are very often used in industry, especially when speed of the response is not an issue. Deceleration of response can be seen from transfer function of integrator shown in Fig. 1.16



(a) Transfer functions of integrator



(b) PI controller transfer function

Fig.1.16: Transfer functions of integrator and PI controller

### 8. Simulation Result and discussion

Simulations were performed by using MATLAB SIMULINK and it also helps to confirm the PWM switching strategy. Fig 1.17 shows the MATLAB simulation for boost converter. Fig 1.18 shows the diagram of closed loop of boost converter. Solar M-file coding for MPPT and

PV simulation is given in the Fig 1.19. PDPWM switching strategy used in this paper. It consists of four reference signals are compared with the triangular carrier signal to produce PDPWM switching signals for switches S1-S8. The inverter adopts a full-bridge configuration with an auxiliary circuit. PV arrays are connected to the inverter via a dc-dc boost converter.

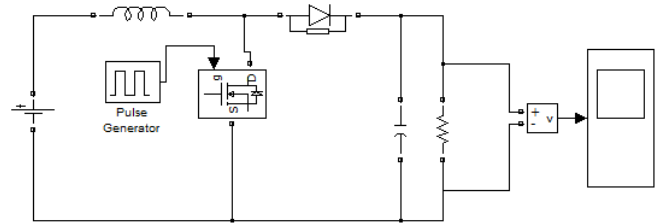


Fig 1.17: Matlab simulation for boost converter

The dc-dc boost converter is used to step up inverter output voltage to ensure power flow from the PV arrays into the load. A filtering inductance  $L_f$  is used to filter the current injected into the load. The injected current must be sinusoidal with low harmonic distortion. In order to generate sinusoidal current, sinusoidal PWM is obtained by comparing a high-frequency carrier with a low-frequency sinusoidal, which is the modulating or reference signal. The carrier has constant period; therefore, the switches have constant switching frequency. The switching instant is determined from the crossing of the carrier and modulating signal. The power circuits for open loop is given in Fig 1.20 and the Power circuit for the closed loop model is given in the Fig 1.21.

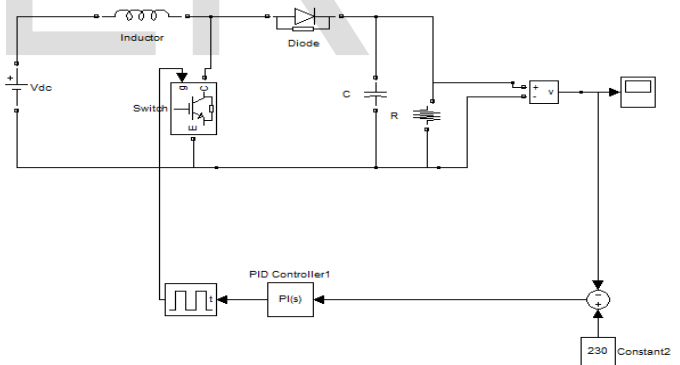


Fig.1.18 : closed loop for the boost converter

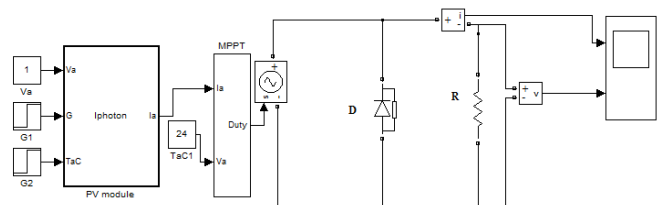


Fig1.19: M-file coding for MPPT and PV simulation

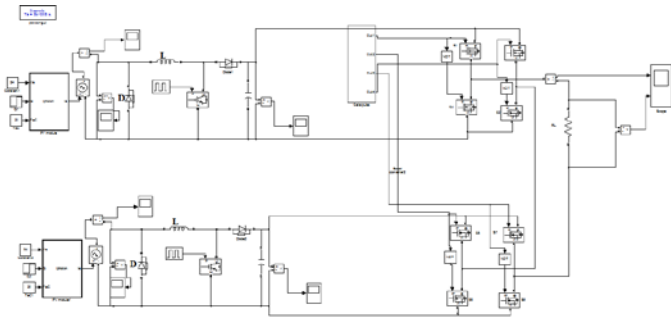


Fig.1.20: Power circuit for open loop

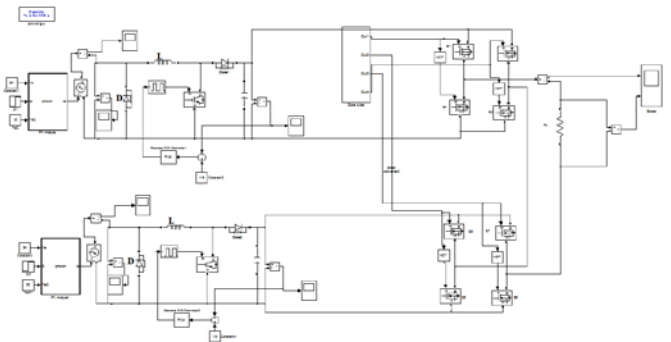


Fig.1.21: Power circuit for closed loop

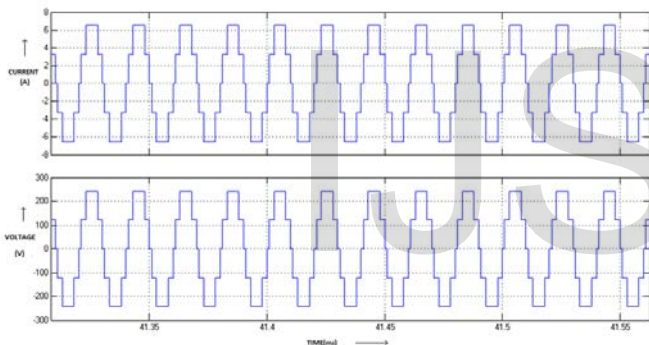


Fig.1.22: Inverter output voltage

The simulated Inverter output voltage ( $V_{inv}$ ) for  $0.5 \leq M \leq 1$ . is shown in Fig 1.22 This output was observed from single phase five-level inverter. The Total Harmonic Distortion for the open loop model is shown in Fig. 1.23.and the THD for the closed loop model is shown in the Fig. 1.24 and the harmonics are reduced from 23.90 to 1.13%.

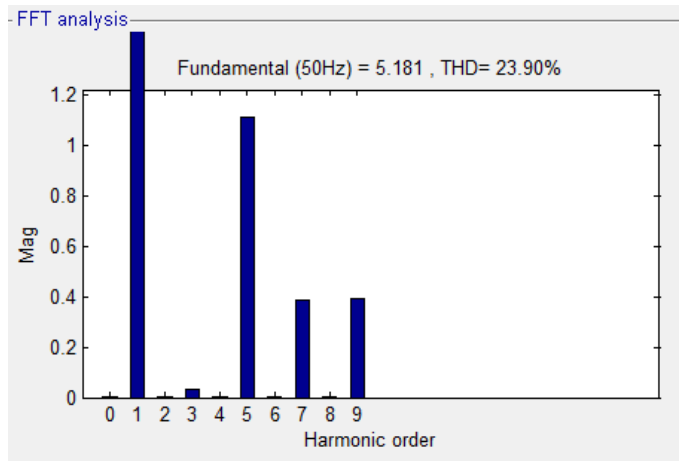


Fig.1.23: THD for open loop mo

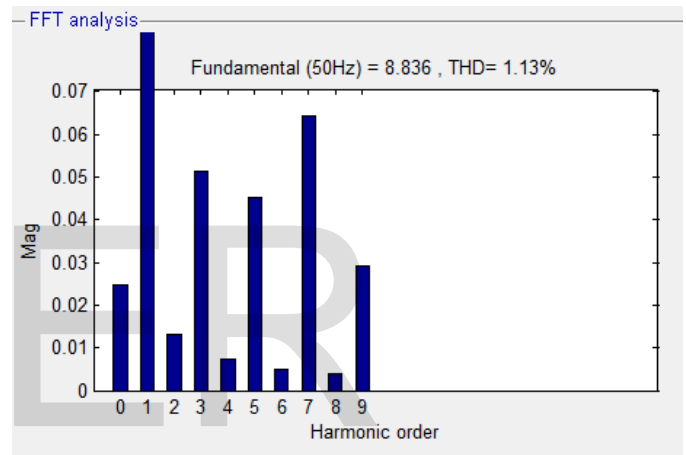


Fig.1.24: THD for closed loop mode

## RESULT

### COMPARISON BETWEEN THD VALUE FOR OPEN LOOP AND CLOSED LOOP MODEL

OPEN LOOP MODEL	CLOSED LOOP MODEL
23.90%	1.13%

#### (1) Analysis of photovoltaic model

Insolation = 1000 w/m<sup>2</sup>  
 Ratings of PV cell (with bypass diode)  
 $V_{oc} = 22.2$  volts,  $I_{sc} = 5.45$  Amp  
 Voltage at  $P_{max} = 17.2$  volts, Current at  $P_{max} = 4.95$  Amp  
 Output dc voltage = 103.2 volts

#### (2) Analysis of boost converter

Input dc voltage = 103.2 volts  
 Inductance ( $L$ ) = 2mH

Load Resistance ( $R_L$ ) = 2K

Output dc Voltage = 235.6

### (3) Analysis of Inverter model

PWM Generation:-

Sampling Time = 2 $\mu$ sec

Modulating Signal:- Modulation Index = 0.8

Frequency = 60 Hz

Input dc signal = 235.6

### (4) Output Signal:-

Carrier Frequency = 1.5 KHz

## 13 Conclusion

This paper presented a single phase multilevel inverter for PV application. It utilizes four reference signals and a carrier signal to generate PWM switching signals. The circuit topology, modulation law and operational principle of the proposed inverter were analyzed in detail. Simulation results indicate that the THD of the five-level inverter is much lesser than that of the conventional three-level inverter.

## 15 References

1. H. S. Bae, S. J. Lee, K. S. Choi and Bo H. Chos. S. Jang, "Current Control Design for a Grid Connected Photovoltaic/Fuel Cell DC-AC Inverter", IEEE Transactions on Energy Conversion, Vol. 24, No. 1, pp. 1945-1950, Mar. 2009.
2. J. Rodriguez, J. S. Lai and F. Z. Peng, "Multilevel Inverters: Survey of Topologies, Controls, and Applications," IEEE Transactions on Industry Applications, Vol. 24, No. 1, pp. 724-738, Aug. 2002.
3. G. Carrara, S. Gardella, M. Marchesoni, R. Salutati and G. Sciotto, "A New Multilevel PWM Method: A Theoretical Analysis", IEEE Transactions on Power Electronics, Vol. 7, No. 3, pp. 497-505, July 1992.
4. Agilities and M. Calais, "Application Specific Harmonic Performance Evaluation of Multicarrier PWM Techniques", IEEE Power Electronics Specialists Conference, Vol. 4, No. 2, pp. 172-178, July 1998.
5. J.-P. Lee, B.-D. Min, T.-J. Kim, D.-W. Yoo, and J.-Y. Yoo, "Design and control of novel topology for photovoltaic dc/dc converter with high efficiency under wide load ranges," Journal of Power Electron. , Vol. 9, No. 2, pp. 300-307, Mar. 2009.
6. H. Bodur and A. Faruk Bakan, "A new ZCT-ZVT-PWM DC-DC converter," IEEE Trans. Power Electron. , Vol. 19, No. 3, pp. 676-684, May 2004.
7. Pompeo Marino and Francesco Vasca, "A New Nonlinear Feedforward Compensation for Feedback Controlled DC-DC Converters," IEEE Power Electronics Specialists Conference, Vol. 4, No. 2, pp. 728-734, June 1993.
8. H. S. Bae, J. H. Yang, J. H. Lee and Bo H. Cho, "Digital State Feedback Current Control using the Pole Placement Technique And the 42V/14V Bi-Directional DC-DC Converter Application," The Applied Power Electronics Conference and Exposition 2007, Vol 3, No. 6, pp. 03-07, Feb. 2007.
9. R. Gules, J. De Pellegrin Pacheco, H. L. Hey, and J. Rnhoff, "A maximum power point tracking system with parallel connection for PV stand alone applications," IEEE Trans. Ind. Electron. , Vol. 55, No. 7, pp. 2674-2683, Jul. 2008.
10. F. Liu, S. Duan, F. Liu, and Y. Kang, "A variable step size INC MPPT method for PV system," IEEE Trans. Ind. Electron. , Vol. 55, No. 7, pp. 2622-2628, Jul. 2008.
11. Chien, K.L., Hrones, J.A., Reswick, J.B., "On the automatic control of generalized passive systems", IEEE Trans. ASME, Vol. 55, No. 7, pp. 26-36, July 2007.
12. Jaeho Lee, Hyunsu Bae and Bohyung Cho, "Advanced Incremental Conductance Mppt Algorithm With A Variable Step Size," 12th International Power Electronics and Motion Control Conference EPE-PEMC, Vol. 65, No. 6, pp. 603-607, Aug. 2006.
13. R. H. Baker and L. H. Bannister, "Electric Power Converter," U.S. Patent 3, Feb. 1975.
14. C. Govindaraju and Dr. K. Baskaran, "Optimized Hybrid Phase Disposition PWM Control Method for Multilevel Inverter", International Journal of Recent Trends in Engineering, Vol 1, No. 3, pp. 129-134, May 2009
15. B.P. Mcgrath and D.G. Holmes "Multi carrier PWM strategies for multilevel inverter" IEEE Transaction on Industrial Electronics, Volume 49, No 4, pp 858-867, Aug 2002.
16. Leon M. Tolbert and Thomas G. Habetler "Novel multilevel inverter carrier based PWM method" IEEE Transaction On Industry Application "Vol 35 No 5, pp 1098-1107, Sep 1999.
17. Kjaer S. B., Pedersen J. K. and Blaabjerg F., "A review of single-phase grid connected inverters for photovoltaic modules," IEEE Transactions on Industry Applications, Vol. 41, No. 5, pp. 1292-1306, Sept.-Oct. 2005.
18. yson Den Herder, "Design and simulation of photovoltaic super system using simulink", master's thesis in California Polytechnic state University, Vol. 35, No. 4, pp. 23-29, Jul 2006.
19. N. D. Benavides and P. L. Chapman, "Modeling the effect of voltage ripple on the power output of photovoltaic modules," IEEE Trans. Ind. Electron., Vol. 41, No. 5, pp. 2638-2643, Jul. 2008.
20. Application Report Understanding Boost Power Stages in Switchmode Power Supplies, TI Literature Number SLVA061, 1999.